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Multilevel cascaded three-phase inverter with low-voltage ride-through flexible control capability for photovoltaic systems

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Abstract. A potential solution for medium and large-scale solar power plants connected to a grid is the multilevel cascaded H-bridge (CHB) inverter. Nevertheless, it has not been thoroughly studied how it operates during voltage sags. An easy strategy for controlling the operation of solar grid-connected CHB inverters in periods of unstable voltage sags is presented in this paper. The main contribution of this study is the fact that the proposed strategy is capable of infusing both reactive power, which represents the so-called low-voltage ride-through capability (LVRT), and active power into the grid with either stable or unstable currents, as well as maintaining voltage balance of all DC-link capacitors. To obtain gate signals, phase-shifted sinusoidal pulse width modulation (PWM) technique is applied. Under various unbalanced voltage sags, the performance of the proposed strategy for the operation of a grid-connected CHB converter was illustrated and validated through a computer simulation platform. Moreover, an experimental setup for a 5-level CHB inverter using MOSFET switches with 5 kHz switching frequency was implemented to reveal the effectiveness of the proposed strategy. The Texas instrument DSP C2000 micro-controller TMS320F28335 was used to detect control, modulation and protection functions in real time and simultaneously. The developed system was tested under severe and light unbalance conditions, and the results show that this system can handle a single-phase voltage sag and be used as a practical device for AC grids.

Key words: power electronics, photovoltaic systems, multilevel cascaded H-bridge inverter, asymmetric voltage sag, low-voltage ride-through.

1. INTRODUCTION

The multilevel inverter has recently become an attracting solution for mainly medium and large-scale Photovoltaic (PV) power plants because of its higher power transfer capability with lower switching frequency, lower total harmonic distortion (THD), lower voltage rating for the switches, and the ability to connect directly to medium voltage, which eliminates the need for bulky transformers. Even though there are a number of multilevel inverter topologies, the cascaded H-bridge (CHB) inverter shown in Fig. 1 is one of the best solutions for the following reasons [1–7]:

- small number of switches, which reduces the semiconductor losses
- easy to increase the number of the output voltage levels
- independent maximum power point tracking (MPPT) capability due to the availability of multiple DC-links.

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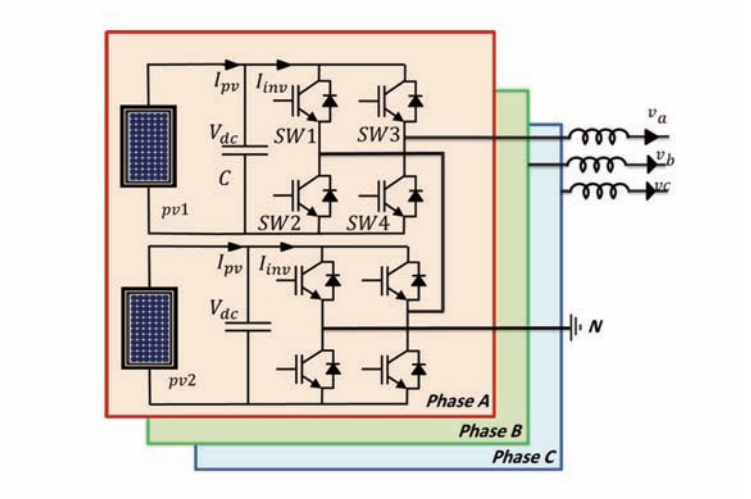

Fig. 1. Cascaded H-bridge 5-level inverter.

Due to partial shading or unbalanced load, each phase of the CHB inverter may generate a different amount of power and experience the phase imbalance issue [3]. These imbalances can lead to:

- drop in the voltage quality
- deviation in one of the DC-link voltages, which may lead to the activation of the over-voltage protection relay or loss of MPPT in case of the single stage power conversion system.

Considering the issues highlighted above, the relevant literature introduces numerous algorithms for stabilizing the current injected to the grid in various conditions. Several zero-sequence voltage injection techniques have been presented for balancing the current injected to the grid during DC side instability due to partial shading [3,8–10]. Yu et al. [11] address the stable current injection when some of the bridges of the CHB inverter experience failure. These studies are mainly concerned with the zero-sequence voltage injection for attaining inter-phase stability, and providing the grid with active power (P) and stable currents under the normal operating condition. Townsend et al. [4] offer a new grid-connected PV power plant topology where the CHB inverter is connected to DC-DC converters, which provides the stable current injection during partial shading and minimizes the second harmonic oscillation of DC-link voltage. The application of bridge voltage modification references to balancing among bridges is also illustrated in [9,12]. These studies examine the operation of the CHB inverter under normal grid operation with active power injection and balanced voltages.

Due to unstable phase currents, inter-phase imbalance is experienced by a grid-connected PV CHB inverter during unstable voltage sags, and uneven power generation from the PV strings (in accordance with the solar irradiance conditions) can further lead to the simultaneous occurrence of imbalances among bridges and inter-phase imbalances. Therefore, there are discussions over various strategies that would achieve low-voltage ride-through capability for the CHB-based static synchronous compensator [13,14]. In addition, Chen et al. [15,16] also consider negative-sequence and zero-sequence current injection of the cascaded H-bridge based static synchronous compensator under grid disturbance circumstances. The major limitation regarding these studies is that they only implement reactive power injection on the grid-connected inverter, whereas synchronized active power injection with either stable or unstable currents from grid-connected PV inverters is also required in modern grid codes [17,18]. Furthermore balancing among bridges and phases should also be taken into consideration. Thus, a flexible control strategy for balancing the DC-link voltage and regulating the active and reactive power of the grid-connected PV CHB inverter is needed, especially during voltage drops. Nonetheless, there is no indication in the relevant literature [1,12,16,19] of any investigation conducted in this regard.

Considering the data in the literature that asymmetric voltage dips occur more frequently than symmetric voltage dips [20,21] and with regard to the foregoing discussion, this study proffers a flexible strategy for controlling the operation of the grid-connected PV CHB inverter during asymmetric voltage drops. It is

well known that when asymmetric voltage dips occur, not only positive-sequence components occur but also negative- and zero-sequence components are observed in the system [3,8–10,16]. For this reason, when designing the controller of the system, the decoupled double synchronous reference frame theory should be considered and references need to be obtained for both positive- and negative-sequence components. The developed strategy has the ability to balance DC-link voltages, as well as the voltage at the point of common coupling (PCC) by deploying the LVRT capability during the disturbances of the load.

Simulations involving a 264 kVA grid-connected 5L-CHB inverter have been used to evaluate and validate the capability and performance of the proposed control strategy on the operation of the grid-connected CHB inverter during voltage drops. Balanced voltage drops are less common than unbalanced voltage drops, and it is also easier to manage the operation of the PV CHB inverter under balanced voltage drops. Hence, while all the case studies examined in this paper are focused on unbalanced voltage drops, the proffered control mechanism can also be applied during stable voltage sags or normal grid operation. Although it is not the primary objective of this study, MPPT can be used consistently for those operations. Moreover, an experimental setup was implemented to validate the controller effectiveness. The experimental setup of CHB was implemented with MOSFET switches and 5 kHz switching frequency. The implemented DSP C2000 micro-controller based CHB inverter figures out control, modulation and protection functions in real time and simultaneously. The developed device was tested under severe and light unbalance conditions and the results of the case studies show that this system can handle a single-phase voltage sag and be used as a practical device for AC grids.

This paper is structured as follows. Section 2 provides an outline of the controlling techniques for the PV CHB inverter connected to the grid. Section 3 reveals the results of the simulations and Section 4 focuses on the experimental setups. Section 5 presents the conclusion.

2. CONTROLLING TECHNIQUE FOR PV CHB INVERTERS CONNECTED TO THE GRID

Figure 1 illustrates the grid-connected PV system configuration with 5L-CHB inverter. A PV power plant equipped with a grid-connected CHB inverter is comprehensively described in [3,8,10]. This section focuses on the N-level CHB in an attempt to generalize the proposed technique. Sections 3 and 4 present the structure of the proposed control technique.

2.1. Synchronous reference frame-based theory (SRF)

According to this method, symmetrical three-phase voltages or currents are transformed into direct, quadrature and zero-sequence components by using power invariant transformation in a synchronously rotating frame and by the agency of the transformation matrix T given in (1), also known as Park Transformation Matrix [22]. The rotating frame is used to synchronize the phase angle of the AC utility voltage with the support of a phase-locked loop. The direct and quadrature components are symbolized by active and reactive components of the system. Although the main aim is to obtain DC quantities in a rotating frame, higher-order harmonics will remain if there are harmonics in the phase voltage or current. Basically, this transformation is first determined by using the transformation matrix C (Clark transformation) given in (2) to find alpha, beta and zero components, and then by synchronizing the phase angle Θ of the AC utility voltage, dq and zero components are calculated.

$$T = \begin{bmatrix} sin(\theta) & -cos(\theta) & 0 \\ cos(\theta) & sin(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix}, \tag{1}$$

$$C = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}. \tag{2}$$

By calculating the three-phase voltages v_0, v_α, v_β, v_d and v_q by means of the transformation matrices T and C given in (1) and (2), transformation can be performed by applying (3) and (4).

$$\begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}, \tag{3}$$

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \begin{bmatrix} sin(\theta) & -cos(\theta) & 0 \\ cos(\theta) & sin(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix}. \tag{4}$$

Here v_0 is the voltage zero component of the two-axis system in the stationary reference frame, v_α the x-axis voltage in the stationary reference frame and v_β the y-axis voltage in the stationary reference frame.

2.2. Pulse width modulation generation

To calculate the d-axis current reference (i_d^*), the error between bridge DC voltage reference v_d^* and $\bar{v}_{dc}$ is fed into a PI controller, as shown in Fig. 2. A sag detection based on an orthogonal system is applied in this study for the calculation of the amplitude of phase voltages and determination of the minimum phase voltage amplitude. The current reference of the q-axis (i_q^*) is determined from the grid codes based on the voltage sag amplitude.

Figure 2 illustrates the current reference calculation design of a PV plant with a CHB inverter connected to a grid in the dq-frame. Based on the grid codes, the reactive current reference is determined by including the grid voltages at PCC $v_{pcc-abc}$ in the calculation algorithm of the current reference, while the active current reference is also calculated by measuring the DC-link voltage. The output of the current reference calculation block are the active power reference current i_d^* and the reactive power reference current i_q^*, which are used for the LVRT capability.

The phase-locked loop (PLL) and the measurement of the abc voltage and current is shown in Fig. 3. The voltage at PCC $v_{pcc-abc}$ and the current at PCC $I_{pcc-abc}$ are measured and converted to the stationary reference frame ($\alpha\beta$ frame). After that Park transformation is used to generate the rotational reference dq-frame v_d, v_q, i_d and i_q. From the active power reference current i_d^*, the reactive power reference current i_q^*, v_d, v_q, i_d and i_q is generated and then the required SPWM will be generated, as described in Fig. 4.

Controlling of i_d leads to regulating the active power. By controlling the active power injected from the CHB inverter, the average DC-link voltage ($\bar{V}_{dc}$) is maintained. The formula (5) for calculating the average DC-link voltage $\bar{V}_{dc}$ is given as:

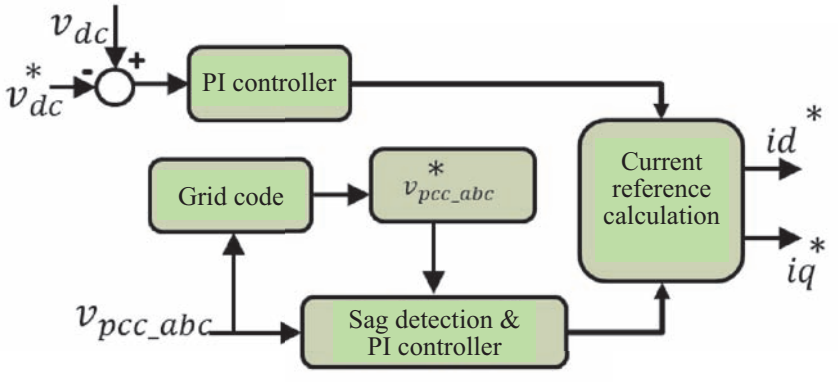

Fig. 2. Current reference calculation.

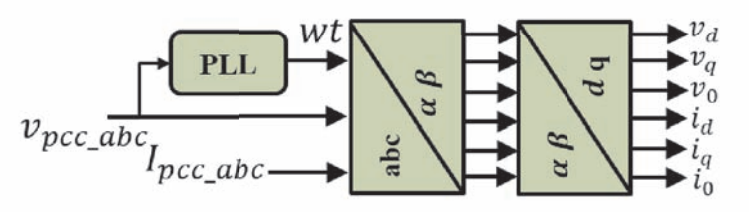

Fig. 3. Converting the measured current and voltage to dq-frame.

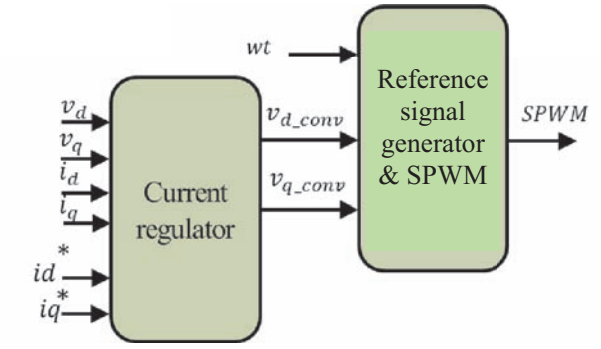

Fig. 4. Current regulator and SPWM.

$$\bar{V}_{dc} \triangleq \frac{\sum_{x=a}^{c}\sum_{j=1}^{N} v_{dc-xj}}{N \times 3}, \tag{5}$$

where $x \in \{a,b,c\}$ phases, j represents the bridge number, the DC-link voltage of bridge xj is represented as v_{dc-xj}, N-levels in each phase and $\triangleq$ means equal to by definition.

In an attempt to illustrate the flexibility of the proposed algorithm, this study provides two distinct strategies for calculating current references: 1) achieving zero active power oscillation through unstable current during unstable voltage sags, as seen in [23]; 2) enhancing PCC during voltage sags by using the inverter's full current capacity whenever there are balanced or unbalanced voltage sags, as given in [24]. Several frame transformations are usually required for implementing the conventional PI controller for injecting balanced currents, which often reduces dynamic performance in contrast with controllers that apply the ABC-framework [25]. Nevertheless, the conventional PI controller is still simpler to implement compared to other types of controllers. The sinusoidal structure of the output voltage reference is preserved by the controlling loops. Moreover, the computational complexity increases due to the need to calculate both negative- and positive-sequence voltages in dq-frame in order to obtain the precise unbalanced current injection under unstable voltage sags [25].

2.3. Feedback voltage compensation impacts

To improve the operation of the controller, voltage sags need to be quickly detected [26]. At the start of voltage sags, there is a high transient current due to the algorithm's delay in detecting voltage sags. This is because the grid keeps receiving maximum power from the controller in the time period from the occurrence of the voltage sag until it is detected. As a result, reducing the transient current during such periods requires the implementation of a feedback voltage compensator. Figure 2 shows the application of a feedback voltage compensator in accordance with [25]. Clark transformation in (2) is first used to convert the instantaneous PCC voltages to the ($v_{pcc-\alpha}$, $v_{pcc-\beta}$ and v_{pcc-0}) $\alpha\beta 0$ reference frame, and then to the $dq0$ reference frame as illustrated in Fig. 3. In the absence of this feedback compensator, it is necessary to stress that the current

controller, which is unable to react immediately to the voltage sag, is completely responsible for regulating the voltage references.

During a balanced or unbalanced voltage sag, utility voltage must remain stable due to the fact that the 5-level CHB inverter must inject an amount of reactive power to the grid to increase the voltage level at PCC. It means that the power factor correction and voltage regulation cannot be achieved together. For this reason the three-phase 5-level CHB inverter will work in the voltage regulation mode. The first stage of this regulation as a very important procedure is detection of the voltage sag type. A symmetric voltage sag can be detected by using Park transformation in (1) and the produced reactive power might be equally injected for each phase. But during an asymmetric voltage sag, a negative-sequence voltage component will occur on PCC and to detect this component, Park transformation can be used again with negative angular frequency. A balanced voltage sag has to be detected and reference current produced to prevent the voltage sag.

2.4. Strategy for inter-phase and inter-bridge stability

As demonstrated in Fig. 5, the addition of the voltage references (v^*_{a-1} , v^*_{b-1}, and v^*_{c-1}) to a zero-sequence voltage (v^*_{zero}) is used as an inter-phase balancing technique. To get high-quality output voltages, all the DC-link voltages of the various phases must be equal. If the power of the bridges of each phase is different, it means that their voltages are different since their currents are equal. To calculate the voltage reference associated with each bridge, the desired deviation of the voltage reference of each bridge for inter-bridge balancing (Δv_{xj}) is added to the value obtained when the voltage reference of the phase (v^*_{a-3}) is divided by N.

3. SIMULATION SETUP AND RESULT

A model was developed by using a computer simulation platform. The circuit includes: a PV source, a 5-level inverter, a controller, a local load, a transformer and a grid as illustrated in Fig. 6. Compared with L and LC types of filters, the *LCL* filter was chosen due to its better service advantages, such as low voltage drop owing to small inductors, better harmonic attenuation performance, limited inrush current of the capacitor and converter robustness under varying grid reactance [27]. Hence, a *LCL* filter was inserted between PCC and the 5-level CHB inverter. For the selected 5 kHz switching frequency, the *LCL* filter parameters were designed as L_i=300 uH, L_g=100 uH and C_f=100 uF to prevent over-amplification and attenuate switching harmonics. The reactor sizes in the *LCL* filter were chosen such that no resistance was needed for damping. L_i denotes the inverter side inductance, C_f represents the filter capacitor and L_g indicates grid side inductance of the *LCL* type of filter. Whole resistances were neglected in this study. While V_{sa}, V_{sb}, V_{sc} illustrate secondary side of the distribution transformer, L_s represents grid inductance.

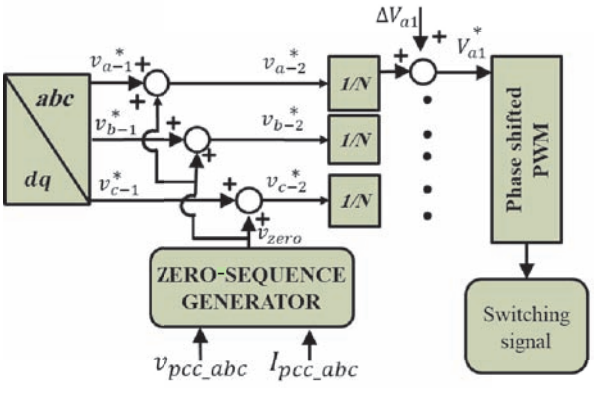

Fig. 5. Inter-phase and inter-bridge voltage regulation.

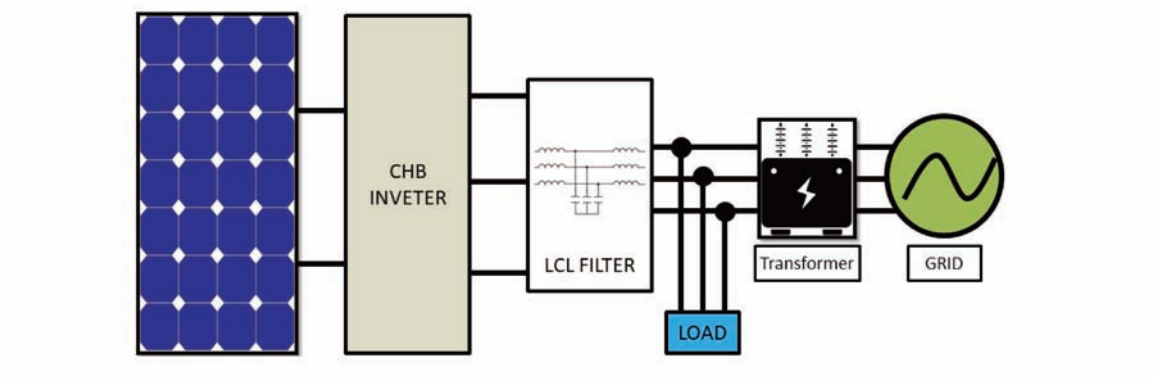

Fig. 6. PV grid-connected model developed in a computer simulation platform.

In the simulated cases below, the inverter controller fixed the DC V_{ref}. To achieve the robust LVRT strategy, the reactive power dispatched to PCC from the PV source has to be calculated carefully. The equation used to calculate the desired amount of reactive power to regulate the voltage is shown in (6):

$$Q = V_{alcl}\frac{V_{alcl} - V_{blcl}}{X_{\Delta}}, \tag{6}$$

where Q is the possible injected reactive power during a voltage sag, V_{alcl} RMS line-to-neutral voltage after the *LCL* filter, V_{blcl} RMS line-to-neutral voltage before the *LCL* filter and X_{Δ} is the reactance between V_{blcl} and V_{alcl}. According to Eq. (6), if V_{blcl} is equal to V_{alcl}, reactive power generation is zero. In order to get the desired V_{blcl} at the terminals of the inverter, the DC voltage V_{dc} was calculated based on the equation (7)

$$V_{dc} = \frac{V_{blcl} * 2 * \sqrt{2}}{\sqrt{3}}. \tag{7}$$

V_{dc} is the DC voltage for each phase, thus half of it for each bridge. So, if the required V_{blcl} is 600 V, it is important to design such a PV power plant that the PV panels would be connected in such a way that it amounts to generating 1000 V DC. In order to generate voltage with five inverter levels, the pulses of each switch have to be generated properly. In this study CHB was chosen for its simplicity and effectiveness. In CHB there are two bridges in each phase and four switches in each bridge. The generated SPWM is indicated in Fig. 7. The figure shows the switching pulses for the positive switches. It is well known that each of the two switches located above each other (e.g. SW1 and SW2 in Fig. 1) need to have the opposite pulses in order to avoid short circuit condition if two switches in one line are turned on simultaneously.

In this research a current controller was realized in synchronous reference frame for generating reference signals which are further used to produce switching signals. After the generated pulses (shown in Fig.7) are involved in controlling the MOSFET switches, the voltage at the output of the inverter is illustrated in Fig. 8. The line-to-ground voltage is depicted in the upper part of the figure (five levels), while the line-to-line voltage is shown in the lower part of the figure (seven levels). The signals reveal the effectiveness of the generated PWM.

The voltage of the system after using the filter is demonstrated in Fig. 9. At the initial condition the peak voltage was regulated at 340 V (240 V rms). At 0.2 s a symmetrical voltage sag occurred, so that the voltages at phases A, B, and C dropped to 300 V peak. Once the controller was enabled at 0.3 s, the voltages at the three phases returned back to the standard value of 340 V. Then, at 0.4 s an asymmetrical voltage sag occurred and the voltage in phase B dropped to 300 V peak. After the controller was active at 0.5 s, the voltage was regulated back to the standard value.

The active and reactive power at PCC is illustrated in Figs 10 and 11. At 0.3 s the controller was enabled to regulate the symmetrical voltage sag. The injection of reactive power was required to stabilize the voltage. At 0.5 s the controller was enabled to regulate the asymmetrical voltage sag as shown in Fig. 11.

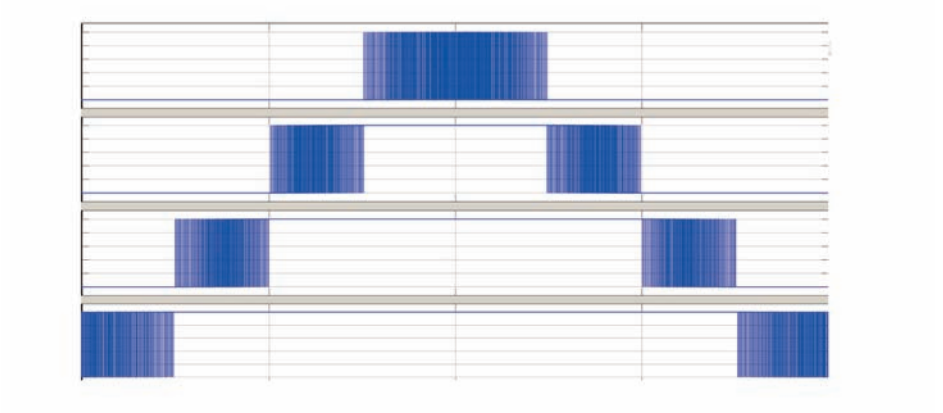

Fig. 7. Positive pulses in each phase to generate 5-level inverters.

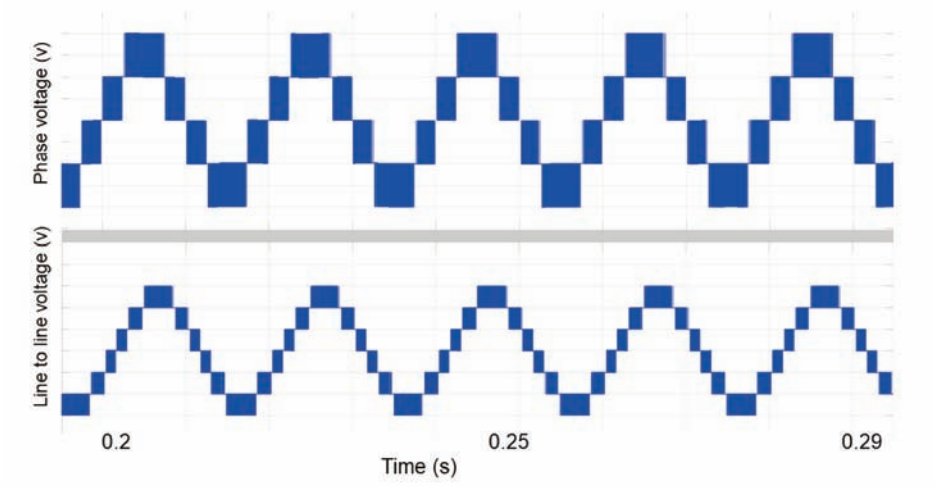

Fig. 8. Inverter's line-to-ground output voltage and line-to-line voltages.

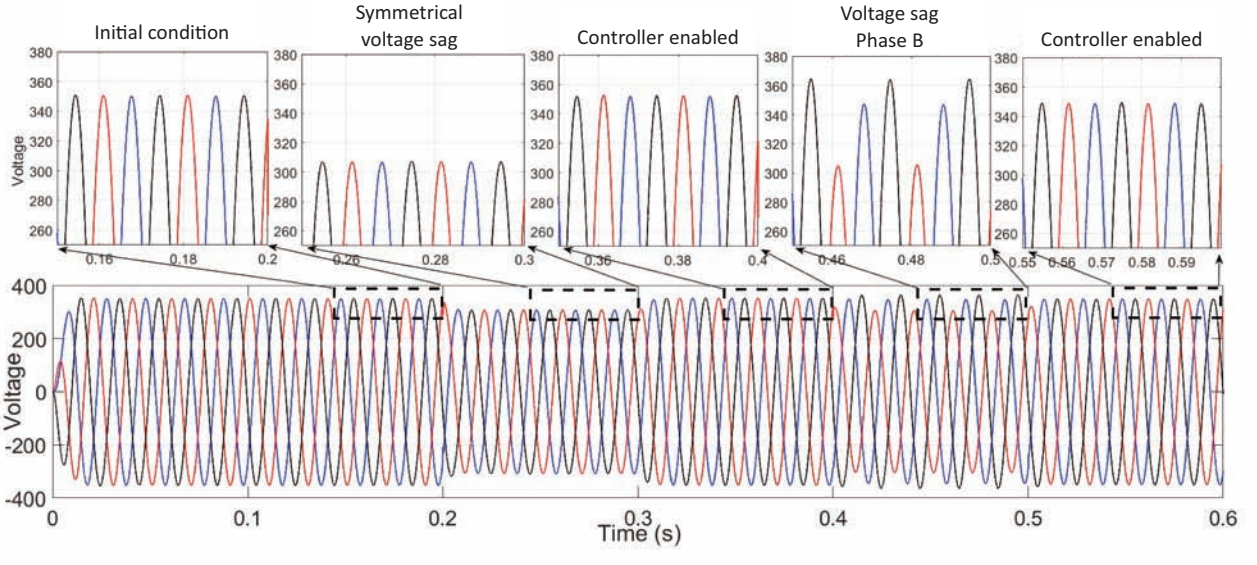

Fig. 9. Voltage after using the filter with symmetrical and asymmetrical voltage sags.

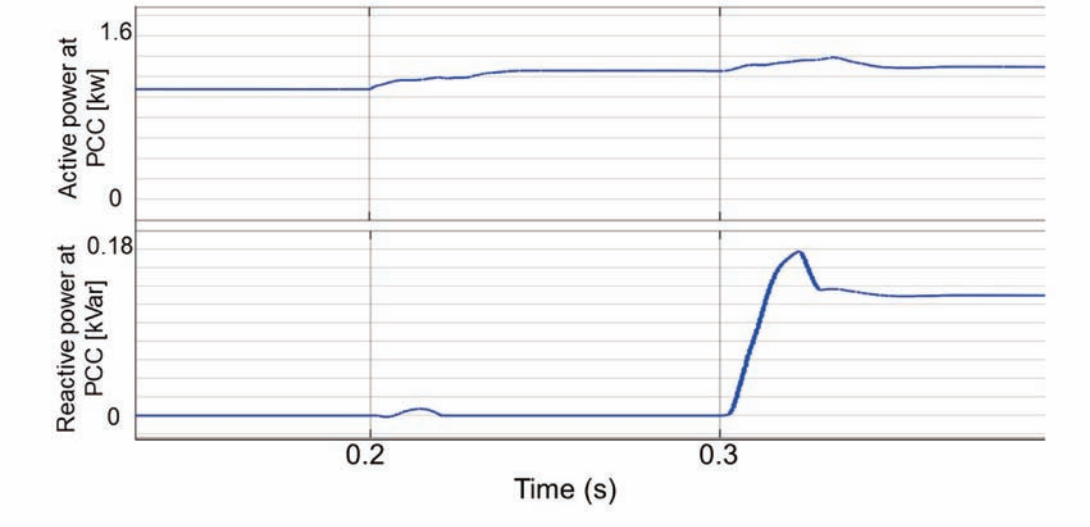

Fig. 10. Active and reactive power at PCC after enabling the controller and injecting Q.

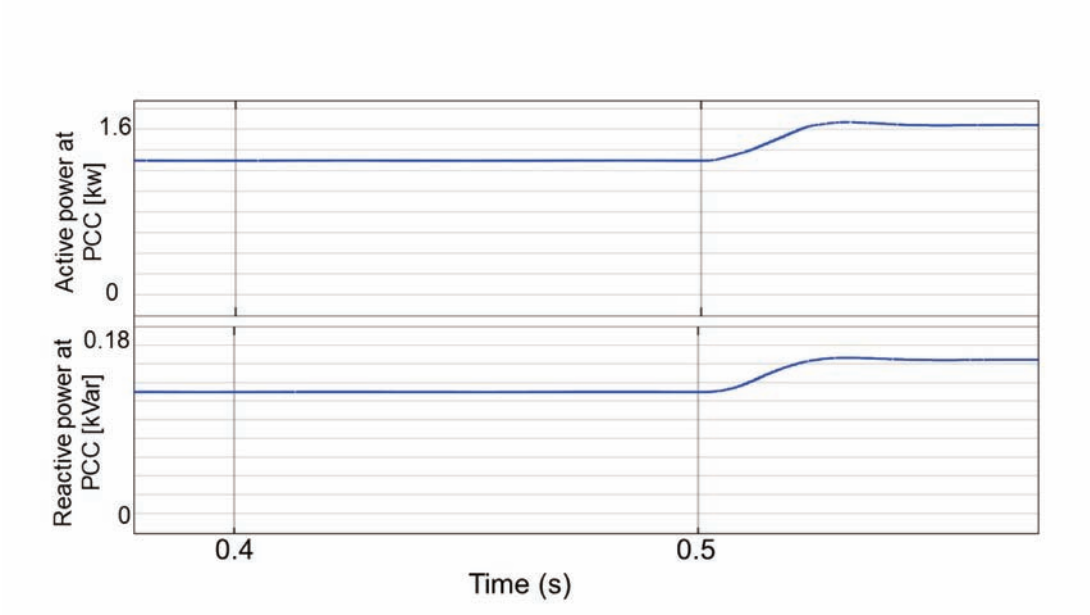

Fig. 11. Active and reactive power at PCC after voltage sag in Phase B.

4. EXPERIMENTAL SETUP

An experimental setup was developed to reveal the effectiveness of the controller. For developing the hardware setup, an electronic design automation software for printed circuit boards (PCB) was used. As illustrated in Fig. 12, there are four switches for each bridge, the voltage at the terminal of each switch is 12 V, and there are three DC-DC converters to supply each bridge. Since the two low-side switches of the circuit have the common grounding, three DC-DC converters are sufficient for this circuit and thus the two switches below are supplied from the same DC-DC converter.

The hardware setup was sampled by the internal 12-bit ADC of the DSP C2000 device. A Hall sensor was used to transfer the current signal into the voltage range of approximately 0 to 5 V with a 0.25 V offset. Then the sensor continued to transfer to the voltage range of approximately 0 to 3 V with the offset, using the resistor divider and external filter and lastly inputting to the micro-controller unit an analog-digital converter. In order to develop the hardware switching circuit, an ePWM module was used. One ePWM module can output two PWM signals with dead-time implementation: EPWMxA and EPWMxB. Six ePWM modules were used to generate 12 PWM signals and then an external NOT gate circuit was developed to generate the opposite signals as shown in Fig. 14. A total of 24 signals were generated from both the C2000 MCU and the NOT gates circuit to drive the three-phase 5-level CHB MLI, by switching the 24 MOSFET switches. Each drive has its own insulated DC-DC power circuit, as illustrated in Figs 12 and 13. PWM pulses were obtained by using a regulating pulse width modulator, an internal soft start and latching. A general block diagram of the hardware module is demonstrated in Fig. 14. This experimenter kit is highly programmable, extremely flexible and simple to use while having the capacity of producing complex pulse width waveforms with reduced CPU overhead or intervention. Each ePWM module has two PWM outputs: ePWMxA and ePWMxB. All ePWM modules in the C2000 device are identical, and more than one module can be used simultaneously to generate synchronized pulses. This module has a high resolution which reaches 159 picoseconds. A built-in dead band sub-module was used to protect the two switches (e.g. SW 1 and SW 2) from being switched on at the same time and creating a short circuit case.

Figure 13 demonstrates the developed circuit for each bridge after mounting the components on the surface of PCB. Each component was chosen carefully to fit properly in the exact location in the circuit. It

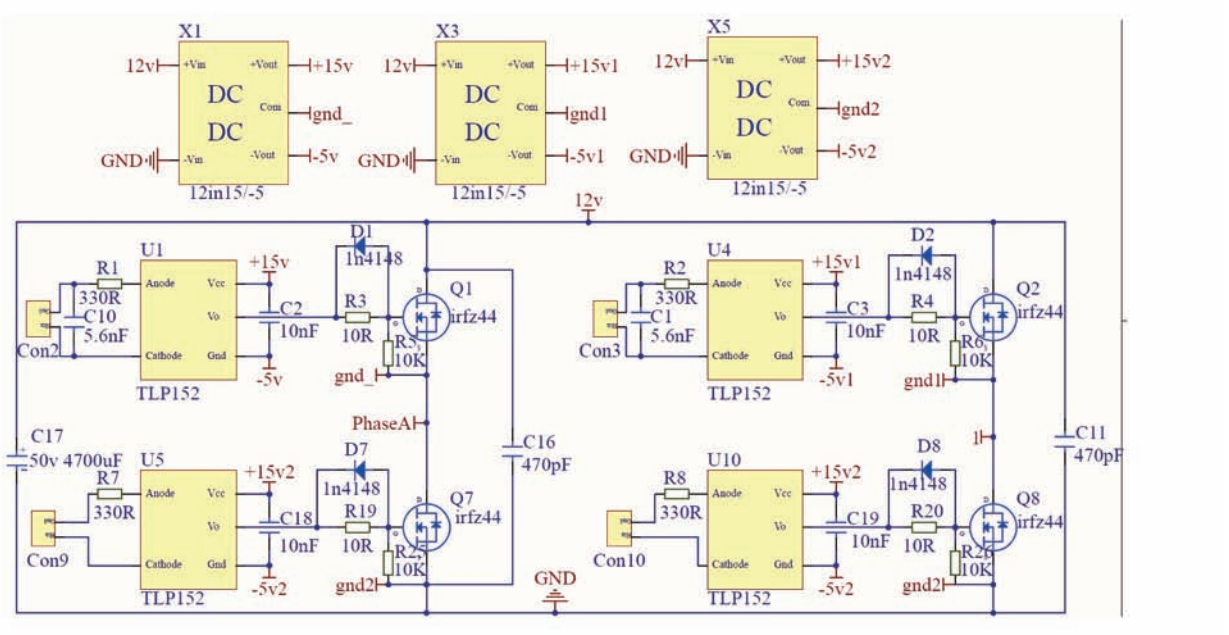

Fig. 12. Circuit diagram of each bridge generated by electronic design automation software.

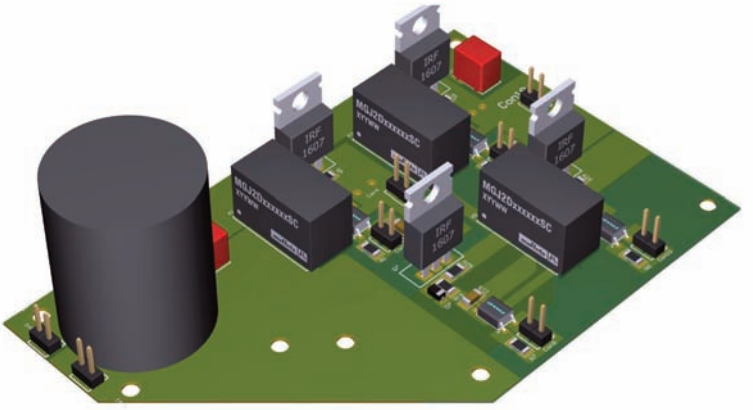

Fig. 13. Circuit diagram of each bridge after mounting the electronic components.

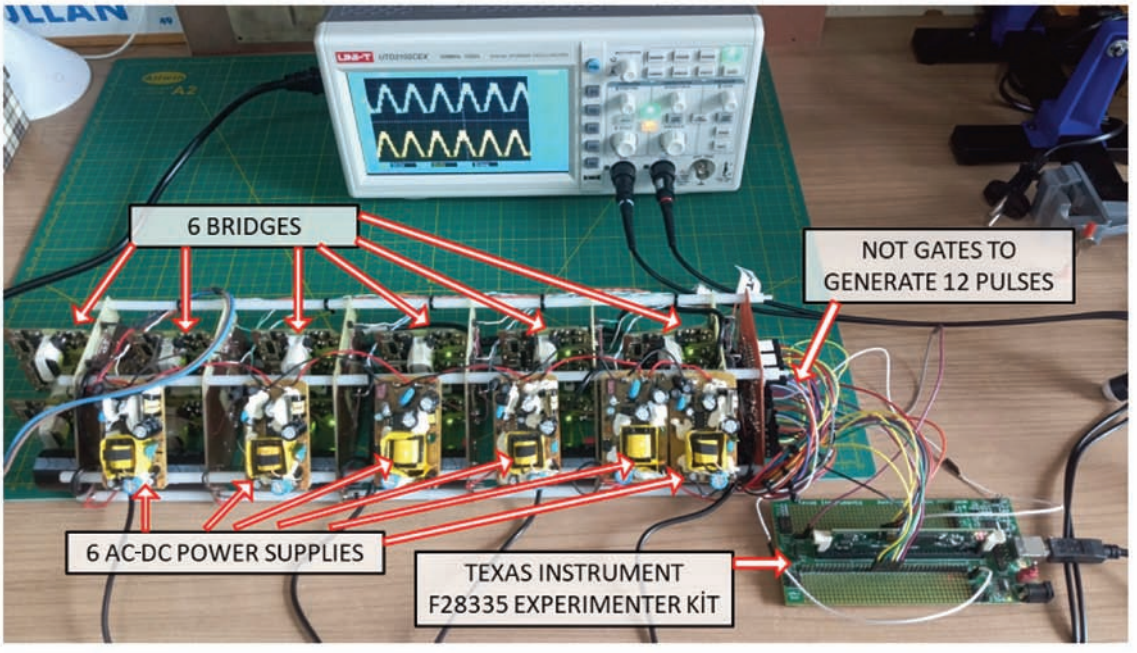

Fig. 14. Hardware setup.

is apparent that there are four switches with three DC-DC converters, and each phase has two circuits (two bridges) as shown in Fig. 1.

The hardware setup was provided with six bridges, two for each phase, and each bridge has four MOSFET switches (see Fig. 14). There are also six AC-DC power supplies for supplying the six bridges. Moreover, the TEXAS INSTRUMENT F28335 EXPERIMENTER KIT was used to generate PWM for the 24 switches. Since the maximum possible output from the TEXAS INSTRUMENT F28335 EXPERIMENTER KIT is 12 pulses, a circuit with 12 NOT gates was used for generating the 12 inverse signals.

An illustration of SPWM is provided by Fig. 15. It can be seen that at the beginning of each pulse there is a short duty cycle, then it is increasing gradually and decreasing again. This creates a smooth sine wave without bulky filter components being required. For any of the two switches above each other (e.g. SW1 and SW2 in Fig. 1) it is very important to avoid having both of them switched on simultaneously as this will create a short circuit situation. Due to this restriction the width of the pulses of SW1 and SW2 has to be the opposite of each other as shown by blue and yellow pulses in Fig. 15.

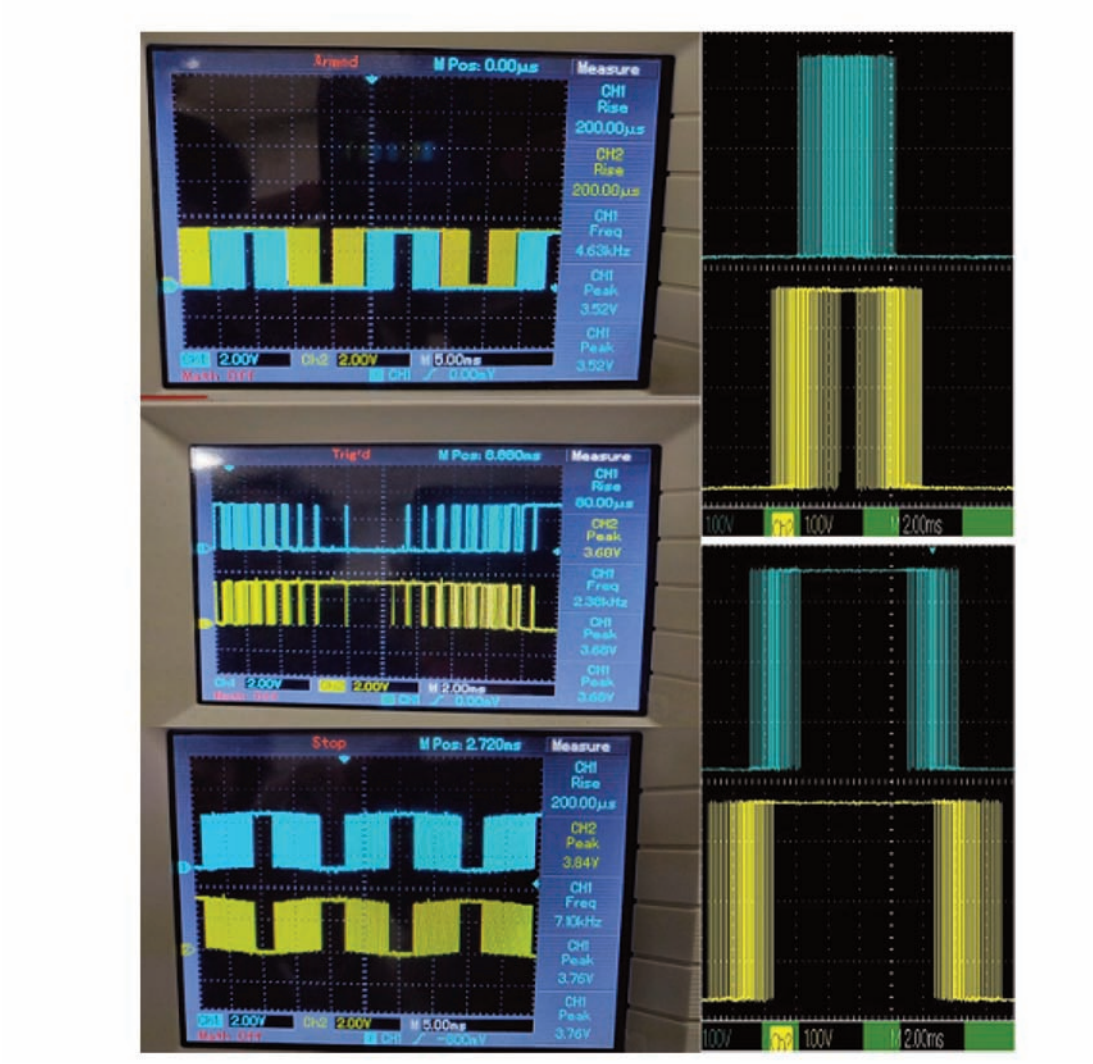

Fig. 15. Sine Pulse Width Modulation to generate smooth sine at the output of the inverter.

The circuit diagram of the gate drive circuit generated by electronic design automation software is shown in Fig. 16. The developed design for the gate drive generates two voltage levels +15 V and –5 V, which makes the MOSFET switches accurate and rapid. The circuit diagram of the gate drive circuit after mounting the electronic components is given in Fig. 17. In order to convert the circuit (demonstrated in Fig. 16) to the final design (shown in Fig. 17), it is very important to place each component in the suitable location. The footprint of each individual part has to be chosen properly. In this study the datasheets of the components were studied and the dimensions were calculated to generate the final shape of the PCB board as shown in Fig. 17. The generated magnetic field from each component was considered during the mounting in order to avoid any interference effect between the components. Also, in the practical circuits proper isolation between high voltage and low voltage regions has to be implemented (DC and AC power circuits and the gate drive circuit). Different separated circuits were used in this research. In addition, the gate drive circuit was placed as close as possible to the MOSFET to avoid gate ringing, parasitic inductance and to keep the frequency distortion as low as possible. The output voltage generated from the hardware setup is presented in Fig. 18. The phase-to-ground voltage shows the five levels. The generated PWM was effective and produced the correct voltage at the output of the inverter.

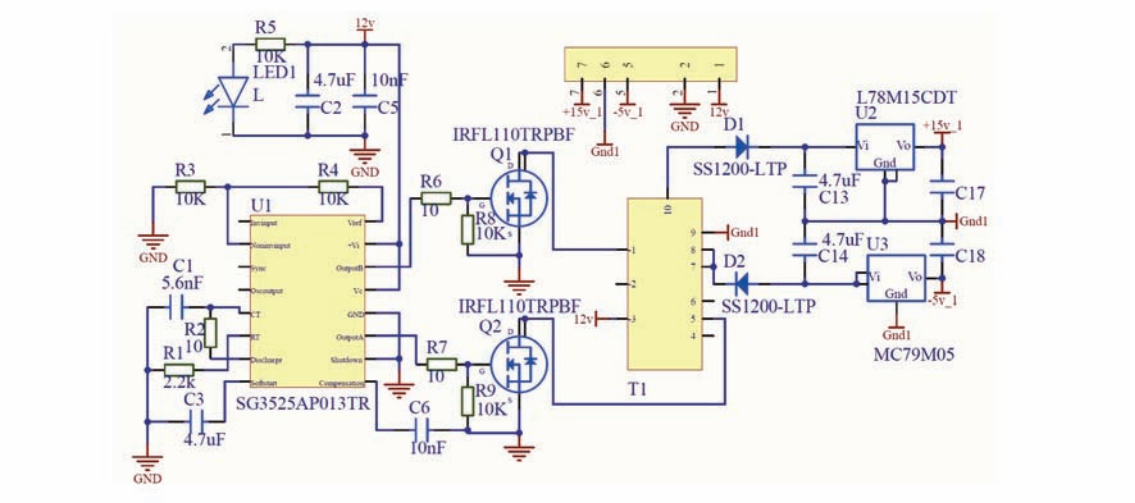

Fig. 16. Circuit diagram of the gate drive circuit generated by electronic design automation software.

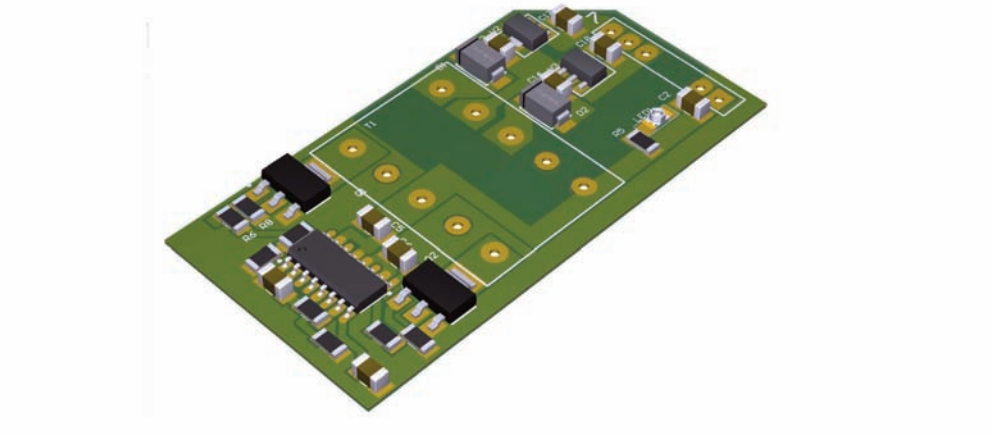

Fig. 17. Circuit diagram of the gate drive after mounting the electronic components.

Fig. 18. Generated voltage in Phase A without a filter.

5. CONCLUSION

During voltage drops, medium and large-scale grid-connected PV power plants require reactive or active power injection. However, no detailed studies have been carried out on the performance of grid-attached CHB inverters which serve as potential candidates for such types of grid-connected PV power plants. In view of that, this paper has introduced a simple strategy for controlling the performance of the solar grid-attached CHB inverter during unbalanced voltage drops. In an attempt to balance the inter-phase voltages, the injection of a zero-sequence voltage was applied while the bridge voltage references were modified to obtain the inter-bridge balancing. A feedback voltage compensator was implemented to significantly reduce the inverter's transient currents at the start of the voltage drop.

Under various unbalanced voltage sag circumstances, a grid-connected PV power plant was used to conduct simulations and experiments in order to determine the effectiveness of the proposed control strategies. Based on the grid codes, the CHB inverter can supply the grid with the right amount of reactive and active power, as well as achieve low-voltage ride-through. Moreover, two distinct current injection techniques were used to verify the proposed controller's flexibility: 1) injecting unstable current without active power oscillation, 2) injecting stable current to enhance the PCC voltage by leveraging the full current capacity of the inverter. The suitability of the proposed control technique for medium and large-scale grid-connected PV power plants in periods of voltage drops was verified by the evaluation results.

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REFERENCES

1. Fuentes, C. D., Rojas, C. A., Renaudineau, H., Kouro, S., Perez, M. A., and Meynard, T. Experimental validation of a single DC bus cascaded H-bridge multilevel inverter for multistring photovoltaic systems. *IEEE Trans. Ind. Electron.*, 2017, **64**(2), 930–934.
2. Sochor, P. and Akagi, H. Theoretical comparison in energy-balancing capability between star- and delta-configured modular multilevel cascade inverters for utility-scale photovoltaic systems. *IEEE Trans. Power Electron.*, 2016, **31**(3), 1980–1992.
3. Yu, Y., Konstantinou, G., Hredzak, B., and Agelidis, V. G. Power balance optimization of cascaded H-bridge multilevel converters for large-scale photovoltaic integration. *IEEE Trans. Power Electron.*, 2016, **31**(2), 1108–1120.
4. Townsend, C. D., Yu, Y., Konstantinou, G., and Agelidis, V. G. Cascaded H-bridge multilevel PV topology for alleviation of per-phase power imbalances and reduction of second harmonic voltage ripple. *IEEE Trans.n Power Electron.*, 2015, **31**(8), 5574–5586.
5. Yu, Y., Konstantinou, G., Townsend, C. D., Aguilera, R. P., and Agelidis, V. G. Delta-connected cascaded H-bridge multilevel converters for large-scale photovoltaic grid integration. *IEEE Trans. Ind. Electron.*, 2017, **64**(11), 8877– 8886.
6. Irusapparajan, G., Periyaazhagar, D., Prabaharan, N., and Jerin, A. R. A. Experimental verification of trinary DC source cascaded H-bridge multilevel inverter using unipolar pulse width modulation. *Automatika*, 2019, **60**(1), 19–27.
7. Annamalai, T., Udhayakumar, K., Anitha, S., Pachaikani, D., Sasikumar, P., and Mythily, M. Energy efficient reference tracking modified enhanced H-bridge multilevel inverter. In *2019 IEEE 1st International Conference on Energy, Systems and Information Processing (ICESIP)*. Chennai, India, July 4–6, 2019, 19228339.
8. Guisso, R., Andrade, A., Hey, H., and Martins, M. d. S. Grid-tied single source quasi-Z-source cascaded multilevel inverter for PV applications. *Electron. Lett.*, 2019, **55**(6), 342–343.
9. Akagi, H., Inoue, S., and Yoshii, T. Control and performance of a transformerless cascade PWM STATCOM with star configuration. *IEEE Trans. Ind. Appl.*, 2007, **43**(4), 1041–1049.
10. Goetz, S. M., Wang, C., Li, Z., Murphy, D. L., and Peterchev, A. V. Concept of a distributed photovoltaic multilevel inverter with cascaded double H-bridge topology. *Int. J. Electr. Power Energy Syst.*, 2019, **110**, 667–678.
11. Yu, Y., Konstantinou, G., Hredzak, B., and Agelidis, V. G. Operation of cascaded H-bridge multilevel converters for large-scale photovoltaic power plants under bridge failures. *IEEE Trans. Ind. Electron.*, 2015, **62**(11), 7228–7236.
12. Ipoum-Ngome, P. G., Mon-Nzongo, D. L., Flesch, R. C., Song-Manguelle, J., Wang, M., and Jin, T. Model predictive current control based on generalised adjacent voltage vectors approach for multilevel inverters. *IET Power Electron.*, 2019, **12**(13), 3590–3599.
13. Xiao, B., Hang, L., Mei, J., Riley, C., Tolbert, L. M., and Ozpineci, B. Modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid-connected applications. *IEEE Trans. Ind. Appl.*, 2015, **51**(2), 1722–1731.
14. Ota, J. I. Y., Shibano, Y., and Akagi, H. A phase-shifted PWM D-STATCOM using a modular multilevel cascade converter (SSBC)â€"part ii: zero-voltage-ride-through capability. *IEEE Trans. Ind. Appl.*, 2015, **51**(1), 289–296.

15. Chen, H.-C., Wu, P.-H., Lee, C.-T., Wang, C.-W., Yang, C.-H., and Cheng, P.-T. Zero-sequence voltage injection for DC capacitor voltage balancing control of the star-connected cascaded H-bridge PWM converter under unbalanced grid. *IEEE Trans. Ind. Appl.*, 2015, **51**(6), 4584–4594.
16. Behrouzian, E. and Bongiorno, M. Investigation of negative-sequence injection capability of cascaded H-bridge converters in star and delta configuration. *IEEE Trans. Power Electron.*, 2017, **32**(2), 1675–1683.
17. Yang, Y., Enjeti, P., Blaabjerg, F., and Wang, H. Wide-scale adoption of photovoltaic energy: grid code modifications are explored in the distribution grid. *IEEE Ind. Appl. Mag.*, 2015, **21**(5), 21–31.
18. Tafti, H. D., Maswood, A. I., Konstantinou, G., Pou, J., and Blaabjerg, F. A general constant power generation algorithm for photovoltaic systems. *IEEE Trans. Power Electron.*, 2018, **33**(5), 4088–4101.
19. Sastry, J., Bakas, P., Kim, H., Wang, L., and Marinopoulos, A. Evaluation of cascaded H-bridge inverter for utility-scale photovoltaic systems. *Renew. Energ.*, 2014, **69**, 208–218.
20. Elphick, S., Smith, V., Gosbell, V., Perera, S., Ciufo, P., and Drury, G. Characteristics of power quality disturbances in Australia: voltage dips at low-voltage sites. *IET Gener. Transm. Distrib.*, 2015, **9**(15), 2382–2388.
21. Ashourpouri, A., Dargahi, M., and Niaki, S. N. Residential voltage dip and swell mitigation using plug-in hybrid electric vehicle in smart grid. In *2013 Australasian Universities Power Engineering Conference (AUPEC)*. Hobert, Australia, September 29 – October 3, 2013, 1–5.
22. Eid, B. M., Rahim, N. A., Selvaraj, J., and Williams, B. W. Electronically coupled distributed generation modeling and control strategies for microgrid applications. *Appl. Math. Inf. Sci.*, 2016, **10**(4), 1343–1353.
23. Naderipour, A., Abdul-Malek, Z., Ramachandaramurthy, V. K., and Guerrero, J. M. Control method for three-phase grid-connected inverter PV system employing unity power factor (UPF) strategy in microgrid. In *E3S Web of Conferences*. Rome, Italy, June 28–30, 2019, Vol. 115, 01006.
24. Roy, A. K., Basak, P., and Biswal, G. R. Low voltage ride through capability enhancement in a grid-connected wind/fuel cell hybrid system via combined feed-forward and fuzzy logic control. *IET Gener., Transm. Distrib.*, 2019, **13**(13), 2866–2876.
25. Jaalam, N., Rahim, N., Bakar, A., and Eid, B. Strategy to enhance the low-voltage ride-through in photovoltaic system during multi-mode transition. *Sol. Energy*, 2017, **153**, 744–754.
26. Tafti, H. D., Maswood, A. I., Konstantinou, G., Pou, J., and Acuna, P. Active/reactive power control of photovoltaic grid-tied inverters with peak current limitation and zero active power oscillation during unbalanced voltage sags. *IET Power Electron.*, 2018, **11**(6), 1066–1073.
27. Arab, N., Vahedi, H., and Al-Haddad, K. LQR control of single-phase grid-tied PUC5 inverter with lcl filter. *IEEE Trans. Ind. Electron.*, 2020, **67**(1), 297–307.